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Filing Date	December 17, 1998
First Named Inventor	Callway
Art Unit	2672
Examiner Name	C. Harrison
Attorney Docket Number	0100.01319

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☑ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Date	March 25, 2005	Reg. No.	34,414

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Callway, et al.	Examiner: C. Harrison
Application No.: 09/213,748	Group Art Unit: 2672
Filed: December 17, 1998	Our File No.: 00100.98.1319
For: METHOD AND APPARATUS FOR INDEPENDENT VIDEO AND GRAPHICS SCALING IN A VIDEO GRAPHICS SYSTEM	Docket No.: 0100.01319

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Christine A. Wright — 3-25-05
Christine A. Wright — Date

TRANSMITTAL OF APPELLANT'S BRIEF PURSUANT TO 37 C.F.R. § 41.37

Transmitted herewith is the Appellant's Brief Pursuant to 37 C.F.R. § 41.37 in this application, with respect to the Notice of Appeal filed on January 28, 2005.

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is $500.00 for a large entity. Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 50-0441. The Commissioner is also authorized to charge any additional fees required by this paper or credit any overpayment thereof to Deposit Account No. 50-0441. A duplicate of this paper is attached.

Respectfully submitted,

Date: March 25, 2005

By: _____
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APPELLANT'S BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Sir:

Appellants submit this brief in furtherance of the Notice of Appeal filed January 28, 2005, in the above-identified application.

I. Real Party in Interest

ATI International, SRL is the real party in interest in this appeal by virtue of an executed Assignment from the named Inventors of their entire interest to ATI Technologies, SRL. The Assignment evidencing such ownership interest was recorded on December 17, 1998 in the United States Patent & Trademark Office at reel number 668, frame 0480.

II. Related Appeals and Interferences

As presently advised, there are no related Appeals or Interferences filed, pending, or decided.

III. Status of Claims

The original Application, number 09/213,748, filed on December 17, 1998, contained original claims 1-37. During prosecution, claims 1 and 5 were cancelled and claim 38 was added. Claims 2, 4, 6-20, and 31-38 were amended. Claims 31-37 are allowed and claims 12-13 and 24-25 are objected to, but would be allowable if rewritten in independent form, including all

of the limitations of the base claims and any intervening claims. Claims 2-4, 6-11, 14-23, 26-30 and 38 are currently rejected under 35 U.S.C. § 103(a). A copy of appealed claims 2-4, 6-30 and 38 is attached in Appendix A below.

IV. Status of Amendments

A "Response to Final Office Action" was filed on October 25, 2004, in which Applicants proposed amending claims 20, 36, 37 and 38 to correct minor typographical errors. In both the Advisory Action mailed January 10, 2005 and the Supplementary Advisory Action mailed January 31, 2005, the Examiner indicated that the aforementioned amendments would not be entered for purposes of appeal. The claims listed in Appendix A reflect the claims as they stood at the time the Final Office Action was mailed on August 25, 2004.

V. Summary of Claimed Subject Matter

The claimed subject matter is generally directed to a method and apparatus for independent video and graphics scaling in a video graphics system. (Specification at 1, ll. 12-14.) More specifically, a video graphics system may include a video graphics display engine or a video graphics display circuit comprising, *inter alia*, a frame buffer, a video scalar, a graphics scalar and a merging block. (Specification at 5-6, Figs. 1-2.)

Figure 1, submitted with the original filing of the present application on December 17, 1998 and reprinted in Appendix B, illustrates a block diagram of a video graphics circuit including, *inter alia*, a frame buffer 10, a video scaler 20, a graphics scaler 30 and a merging block 40. (Specification, Fig. 1.) Among the other benefits the system derives from the frame buffer 10 is the ability of the video graphics system to continually write new data to this memory for display. One of ordinary skill in the art may appreciate that a frame buffer 10 is a buffer. In other words, it, *inter alia*, stores data from another source. A frame buffer itself is not the source of data stored therein. Significantly, the frame buffer 10, in one embodiment, can store video data 12 and graphics data 14 from a source external to the frame buffer 10. (Specification at 5, ll. 3-4.) For instance, as illustrated, the video data 12 may correspond to video data processed by the video engine 16. (Specification at 5, ll. 3-6.) Similarly, the graphics data 14 may correspond to graphics data processed by the graphics engine 18. (Specification, Fig. 1.) In another

embodiment, the disclosure teaches that the video data 12 and graphics data 14 may be received by the video graphics system in a unitary stream. (Specification at 5, ll. 14-17.)

As illustrated, the video scaler 20 is operably coupled to the frame buffer 10 and is adapted to receive therefrom the video data 12. (Specification, Fig. 1.) In response, the video scalar 20 scales the received video data 12 to produce a scaled video data stream 22. (Specification at 5, ll. 21-22.) In one embodiment, the scaling performed by the video scaler 20 is based on a ratio between the eventual display aspect ratio and the aspect ratio of the video data 12 in its current form. (Specification at 5, ll. 23-24.) Similarly, the graphics scalar 30 is operably coupled to the frame buffer 10 and is adapted to receive therefrom the graphics data 14. (Specification, Fig. 1.) In response, the graphics scalar 30 produces a scaled graphics data stream 32 after scaling the received graphics data 14. (Specification at 5, ll. 24-26.) As described above, the scaling may, in one embodiment, be based on a ratio between the eventual display aspect ratio and the aspect ratio of the graphics data 14 in its current form. (Specification at 5, ll. 26-28.)

The merging block 40 is operatively coupled to both the video scaler 20 and the graphics scaler 30 such that it is operative to receive both the scaled video data stream 22 and the scaled graphics data stream 32. (Specification at 5, l. 29 - at 6, l. 2.) Upon receipt of the scaled video and graphics streams 22, 32, the merging block 40 combines the streams to produce a video graphics output stream 42 for display by a monitor or other display device. (Specification at 6, ll. 2-4.) Because the video data 12 and the graphics data 14 are received from the frame buffer 10, independently scaled and later combined to produce a video graphics output stream 42, the circuit illustrated in Figure 1 provides more flexibility than prior art solutions that included only one scaler. (Specification at 6, ll. 4-7.)

Figure 2, submitted with the original filing of the present application on December 17, 1998 and reprinted in Appendix C, illustrates a video graphics display engine that includes, *inter alia*, a frame buffer 110 with first and second memory blocks 112, 114, a video scaler 160, a graphics scaler 170, a merging block 180 with pixel rate adjust block 192 and a graphics decompression block 130. As described in the disclosure, the video graphics display engine is preferably implemented on a single integrated circuit that may contain additional circuitry.

(Specification at 6, ll. 13-14.) However, it is recognized that the video graphics engine may also be implemented through other techniques known in the art. (Specification at 14, l. 27 – at 15, l. 5.)

The frame buffer 110 of Figure 2 may include a first memory block 112 and a second memory block 114 "to store video and/or graphics data" for subsequent display. (Specification at 6, ll. 10-11, Fig. 2.) In addition to merging the scaled video stream 164 and the scaled graphics stream 174, the merging block 180 may include, *inter alia*, a pixel rate adjust block (or circuitry) 192. (Specification, Fig. 2, claims 15-16.) As part of the merging block 180, the pixel rate adjust block/circuitry 192 may, in one embodiment, alter the pixel rate of video graphics output stream 182 such that more efficient scaling of the images of the video data and graphics data streams 122, 132 is possible. (Specification at 8, ll. 26-29.) In one example, the disclosure teaches that this efficiency may be realized, among other ways, by altering the horizontal video pixel rate of the video data stream 122 such that the horizontal portion of the aspect ratio of the output display is equal to a multiple of the horizontal portion of the aspect ratio of the video data streams 122. (Specification at 8, l. 29 – at 9, l. 6.) Additionally, the graphics decompression block 130 serves to decompress the graphics stream 118 from the frame buffer 110 if the graphics stream 118 is in a compressed format. (Specification at 7, ll. 10-12.)

The method of Figure 4, submitted with the original filing of the present application on December 17, 1998 and reprinted in Appendix D, implements *inter alia* the methods described above with respect to Figures 1-2. (Specification, Fig. 4.) That is, the disclosed method allows video data and graphics data to be written to the frame buffer, read from the frame buffer, independently scaled, merged and converted into a display compatible format. (Specification at 12-14, Fig. 4, claim 20.)

Among many benefits, is the ability of the frame buffer memory to be allocated in a flexible and efficient manner such that large blocks of memory are not left idle or wasted. (Specification at 14, ll. 12-14.) Reducing the amount of memory required for either the video or graphics portion of the display has the positive effect of lowering the bandwidth burden on the frame buffer because there is a direct relationship between memory size and the number of required data-read and data-write commands that are necessary to maintain system integrity.

(Specification at 14, ll. 14-18.) In other words, as memory size decreases, so does the number of necessary read/write commands. (Specification at 14, ll. 14-18.) Therefore, the flexible use of the frame buffer and the reduced bandwidth usage allows the system to display images in a more efficient and faster manner. (Specification at 14, ll. 19-22.) Lastly, the method provides a greater number of display options such that a user can utilize, individually or in combination, displays for video data only, displays for graphics data only, or displays for merged video graphics data. (Specification at 14, ll. 21-22.)

VI. Brief Summary of the Prior Art References

A. THE FUJIMOTO REFERENCE

As it is understood, U.S. Patent No. 5,912,710 ("Fujimoto") is directed to an image display control apparatus for, *inter alia*, displaying blended images on a television monitor using source DVD media 100 as the source of the display information. (Fujimoto, col. 1, ll. 15-16, col. 3, ll. 7-18.) In each instance where the source DVD media 100 is referenced, it is described as read-only memory that serves as the source of the display in formation. (*See e.g.,* Fujimoto, col. 5, ll. 7-36, col. 11, ll. 16-41.)

Specifically, Fujimoto teaches a system wherein, the video data 100B and graphics data 100G are read from the source DVD media 100 ("DVD-ROM") by the DVD driver 101 (Fujimoto, col. 5, ll. 27-29) operating under the control of the CPU 11 (Fujimoto, col. 11, ll. 16-19). In this process, the CPU writes the graphics data 100G directly to VRAM 103 (Fujimoto, col. 11, ll. 19-23), a volatile random access memory (Fujimoto, col. 11, ll. 19-23). With respect to the video data 100B, Fujimoto states that "the motion picture [video] data stored in the main memory 13 are provided to the MPEG2 decoder 102 through the [DVD driver] 101." (Fujimoto, col. 11, ll. 33-35.) In other words, Fujimoto clearly explains that while the graphics data 100G are stored directly in VRAM 103 after being read by the DVD driver 101, the video data 100B are first stored in main memory 13, presumably through the use of the internal ISA bus 2a and the host/PCI bridge (Fujimoto, col. 11, 14-35, Fig. 8.) After being stored in main memory 13, the video data 100B are then sent through the DVD driver 101 to the MPEG2 decoder 102. (Fujimoto, col. 11, ll. 33-35.) After storage in the VRAM 103, the graphics data 100G are subsequently scaled by the first scaler 106. (Fujimoto, col. 7, ll. 29-46.) Similarly, after storage in main memory 13, the video data 100B are decoded by MPEG2 decoder 102 and scaled by the

second scaler 107. (Fujimoto, col. 6, ll. 23-27.) In no instance does Fujimoto teach or suggest a system or method for, *inter alia*, a frame buffer that receives a video and graphics data stream and stores the data streams therein.

Importantly, Fujimoto further indicates the importance of using a separate graphics VRAM 103 and main memory 13 in a pipeline (Fujimoto, Fig. 1, elements 103, 104, 155, 108, Fig. 8, element 203, Fig. 9) designed to, *inter alia*, scale graphics data 100G and merge the scaled graphics data with separately scaled video data (Fujimoto, col. 5, ll. 15-27), instead of frame buffer memory (i.e. video memory). Fujimoto directly states that an object of its disclosure is "to provide an apparatus and method for controlling a display of mixed images of graphics and video data on a video monitor by an effective pipeline operation of scaling and filtering the graphics data without using large expensive video memory." (Fujimoto, col. 2, l. 65 – col. 3, l. 2, emphasis added.) Additionally and with respect to the graphics pipeline, Fujimoto also teaches that "it becomes possible to display the graphics on a television monitor 200 with improved quality without using a special and/or large video memory." (Fujimoto, col. 14, ll. 9-24, emphasis added.) In other words, Fujimoto directly criticizes systems that may use larger video memories to store both video and graphics data.

B. THE PORTER REFERENCE

U.S. Patent No. 6,208,354 ("Porter") is directed toward, *inter alia*, storing and displaying multiple graphical images in a mixed video graphics display system. (Porter, Abstract.) Porter appears to disclose a memory 10 capable of storing, *inter alia*, video and graphics data 16, 28. (Porter, Fig. 1.) "Preferably, the memory 10 is a dynamic random access memory that is utilized as a frame buffer within the video graphics circuit." (Porter, col. 2, ll. 54-56.) In operation, the memory 10 directly provides a video data stream 16 and graphics data stream 28 to a display overlay engine 30 having an alpha blend unit 32 to generate the display output signal 35. (Porter, Fig. 1.) In alternate embodiments, Porter discloses that the video data stream 16 may be retrieved from another block within the system other than the memory 10. (Porter, col. 3, ll. 54-57.) Therefore and in at least one embodiment, the memory 10 is in communication with the display overlay engine 30 to provide one or more of the video data stream 16 and graphics data stream 28 thereto. (Porter, col. 3, ll. 52-54.)

VII. Grounds of Rejection to be Reviewed on Appeal

The first issue on appeal is whether claims 2-4, 6-11, 14-23, 26-30 and 38 are patentable under 35 U.S.C. § 103(a) in view of Fujimoto and further in view of Porter.

The second issue on appeal is whether claims 12-13 and 24-25 are patentable over the prior art reference cited.

VIII. Argument

The obvious rejections directed at claims 2-4, 6-11, 14-23, 26-30 and 38 must be reversed because the Final Office Action mailed August 25, 2004 ("Final Office Action") failed to: (1) recognize that Fujimoto explicitly teaches away from any combination with Porter; (2) submit a *prima facie* case of obviousness due to the reliance on broad and conclusory statements of motivation; and (3) demonstrate that each limitation in Applicants' claimed subject matter is taught in the combination of Fujimoto and Porter. More specifically, any combination Fujimoto would be improper since Fujimoto directly teaches against using a video memory to store both video and graphics data received from a source. Furthermore, if a frame buffer were substituted in place of the source DVD-ROM 100 of Fujimoto, Fujimoto's system would be inoperative without a data source of video and graphics data and would have redundant non-source video storage since both the substituted frame buffer and the main memory would both be used Fujimoto according to the rejection. Lastly, because the Examiner has provided only bald statements as to why one of ordinary skill in the art would combine two seemingly incompatible references, the Final Office Action has not established a *prima face* case of obviousness. For these reasons and the ones detailed below, the aforementioned claims are respectively submitted for timely allowance.

A claim is obvious under the Patent Act "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a) (2004). A finding of obviousness, as a preliminary matter, requires a demonstration that the prior art teaches or suggests each claim limitation. LESTER HORWITZ, PATENT OFFICE RULES AND PRACTICE: MANUEL OF PATENT EXAMINING PROCEDURE § 2143.03 (8th ed. 2003); *see also In re Thrift*, 398 F.3d 1357, 1366, 63

U.S.P.Q.2d 2002, 2008 (Fed. Cir. 2002) (reversing a Board's adverse decision on obviousness because the prior art references failed to support each claim limitation).

Because most inventions derive from combinations of "known elements," the possibility that each claim limitation might be separately found in several prior art references is not sufficient to establish obviousness. *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1316 (Fed. Cir. 2000). In other words, the United States Patent and Trademark Office ("PTO") cannot merely employ a reference-by-reference, limitation-by-limitation analysis in rejecting a claim under 35 U.S.C. § 103(a). *In re Dembiczak*, 175 F.3d 994, 1000, 50 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1999). If this were the standard, few, if any, patents would ever issue. *In re Rouffett*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Instead, prior art references must be considered in their entirety to determine whether a skilled artisan, without knowledge of the claimed subject matter, would have combined the identified elements in the manner claimed. *Kotzab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1317. To support a legal determination of obviousness, this Board must address, *inter alia*, the following factual considerations regarding: "(1) the scope and content of the prior art; (2) the level of ordinary skill in the art; [and] (3) the differences between the claimed invention and the prior art. . . ." *Ruiz v. Z.B. Chance Co.*, 234 F.3d 654, 662-63, 57 U.S.P.Q.2d 1161, 1165 (Fed. Cir. 2000).

A. THE OBVIOUS REJECTION MUST BE REVERSED SINCE THE FUJIMOTO REFERENCE TEACHES AWAY FROM THE ALLEGED COMBINATION WITH THE CLAIMED SUBJECT MATTER

During prosecution, the PTO bears the initial burden of providing a *prima facie* case of obviousness. *In re Glaug*, 283 F.3d 1335, 1338, 62 USPQ.2d 1151, 1152 (Fed. Cir. 2002). If a *prima facie* case is properly presented, the burden shifts to the applicant to rebut the PTO's initial determination. *Id.* Patentability *vel non* can only be determined by a preponderance of the evidence and weight of the argument based upon the entire record. *Id.* Because one of the factual considerations relevant to the legal determination of obviousness addresses the scope and content of the prior art, a showing that the prior art materially teaches away from the claimed subject matter is sufficient to overcome the PTO's initial *prima face* case. *In re Peterson*, 315 F.3d 1325, 1331, 65 U.S.P.Q.2d 1379, 1384 (Fed. Cir. 2003).

1. BY CRITICIZING THE USE OF VIDEO MEMORY TO SIMULTANEOUSLY STORE VIDEO DATA AND GRAPHICS DATA, FUJIMOTO TEACHES AWAY FROM THE CLAIMED SUBJECT MATTER

Prior art teaches away from the claimed subject matter when "a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in [applicant's] reference, or would be led in a direction divergent from the path that was taken by the applicant. *In re Gurley*, 27 F.3d 551, 553, 31 U.S.P.Q.2d 1130, 1131 (Fed. Cir. 1994). Prior art may teach away if, for instance, it criticizes, discredits or otherwise discourages the claimed solution. *In re Fulton*, 391 F.3d 1195, 1201, 73 U.S.P.Q.2d 1141, 1146 (Fed. Cir. 2001). "[I]n general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *Gurley*, 27 F.3d at 553, 31 U.S.P.Q.2d at 1131. In this context, each reference must be considered in its entirety. *Kotzab*, 217 F.3d at 1371, 55 U.S.P.Q.2d at 1317.

In *In re Lueders*, the Federal Circuit noted that the claimed subject matter inherently recited a dynamic interactive connection between a keyboard and the display of the invention such that the display was dynamically responsive to the keyboard. 11 F.3d 1569, 1574, 42 U.S.P.Q.2d 1481, 1474 (Fed. Cir. 1997). The prior art, in contrast, taught a pressure-sensitive keyboard with a static display. *Id.* at 1572, at 1483. Upon depression of the keyboard, the prior art device emitted an audio output. *Id.* at 1572, at 1483. As a result, the Court was persuaded that the prior art taught away from the claimed subject matter because all displays in the prior art were "static and only change[d] by manual replacement of the entire display." *Id.* at 1574, 1484.

a. Claims 3, 7, 9, 14, 17 and 19 Stand Together with Claim 4

Because Fujimoto clearly teaches that the use of the disclosed apparatus provides the ability to control "a display of mixed images of graphics and video data on a video monitor by an effective pipeline operation of scaling and filtering the graphics data without using large expensive video memory" (Fujimoto, col. 2, l. 65 – col 3., l. 2, emphasis added), Fujimoto explicitly criticizes and discourages one of ordinary skill in the art from pursuing a display system including a frame buffer that stores both video and graphics information. Fujimoto's teaching point is repeated throughout the disclosure and is followed in each of the embodiments

suggested by the reference. Because one of ordinary skill in the art, after reading Fujimoto, would be "led in a direction divergent from the path that was taken by the applicant," *Gurley*, 27 F.3d at 553, 31 U.S.P.Q.2d at 1131, Fujimoto teaches away from the claimed frame buffer.

As indicated, Fujimoto clearly teaches throughout its disclosure to keep video data 100B separate from video data 100G after being read from the source of the video and graphics data, namely DVD-ROM 100. For instance, Fujimoto describes that, with respect to the graphics pipeline operation of scaling and filtering, "it becomes possible to display the graphics on a television monitor 200 with improved quality without using a special and/or large video memory." (Fujimoto, col. 14, ll. 9-21, emphasis added.) Because each word in a claim must be evaluated under an obviousness evaluation, *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970), an understanding of Applicants' claim limitations is required. Claim 4 requires, *inter alia*, "a single frame buffer . . ., the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block." (Specification, claim 4, emphasis added.) A plain reading of Applicants' claim 4 indicates that both the video data stream and graphics data stream are "fetched from" the memory blocks of the frame buffer. (Specification, claim 4.) In other words, Applicants claim, *inter alia*, the use of a frame buffer, i.e., a type of video memory, to store both video and graphics data. Because the entire Fujimoto reference is based upon avoiding the use of large, expensive video memory, it can hardly be said, therefore, that one skilled in the art, after reading Fujimoto, would not be discouraged from following the path claimed by Applicants.

In fact, the proposition that Fujimoto actually teaches away is supported by the recent *Lueders* holding where the Federal Circuit held, in part, that because the prior art only disclosed embodiments using a static display, the prior art taught away from the claimed dynamic display. 111 F.3d at 1574, 42 U.S.P.Q.2d at 1484. In the present case, not only does the reference criticize systems that incorporate large, expensive memories capable of storing both video and graphics data, but each described embodiment uses separate storage devices for video data 100B and graphics data 100G. In fact, the Final Office Action clearly confirmed Applicants' position when it noted that "Fujimoto's discloses the loading the [sic] media (i.e. graphics and video) data from the DVD; where the graphics data is loaded into VRAM and the video data is loaded into

main memory (col. 11, ll. 15-24)." (Final Office Action at 9.) Because all the embodiments and illustrations described by Fujimoto do not use large, expensive video memories to store both video and graphics therein, the reference must be said to teach away from Applicants' presently claimed frame buffer, a type of video memory operative in Applicants' claim 4 to, *inter alia*, store both "the stream of video data" and "the stream of graphics data (Specification, claim 4).

The only development flowing from Fujimoto's disclosure runs counter to Applicants' claimed subject matter, and therefore is unlikely to be productive of the result sought by Applicant. One of ordinary skill in the art would not be motivated to disregard the express teachings of Fujimoto and use a frame buffer as claimed by Applicants. For the aforementioned reasons, the obvious rejections with respect to claims 3, 4, 7, 9 14, 17 and 19 must be reversed.

b. Claims 22 and 26-28 Stand Together with Claim 20

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 20 requires, *inter alia*, a "method for displaying video graphics data comprising: receiving a video data stream . . . ; allocating a first block of a memory in a frame buffer for storing the video data stream . . ., receiving a graphics data stream . . ., [and] allocating a second block of a memory in a frame buffer for storing the graphics data stream . . . . (Specification, claim 20, emphasis added.) In contrast, Fujimoto expressly criticizes this practice (Fujimoto, col. 2, l. 65- col. 3, l. 2, col. 14, ll. 9-21) and, for the reasons stated above, would discourage one of ordinary skill in the art from following the path described in Applicants' disclosure. Therefore, claims 20, 22 and 26-28 are believed to be allowable for at least the same reasons that claims 3, 4, 7, 9, 14, 17 and 19 are allowable over Fujimoto in view of Porter.

c. Claim 30 Stands Independently

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 30 requires, *inter alia*, a "video graphics integrated circuit comprising: a frame buffer, wherein the frame buffer stores video data and graphics data . . . ." (Specification, claim 30, emphasis added.) Applicants respectfully note that claim 30 explicitly recites a frame buffer, as indicated above, that stores video data and graphics data. In contrast, Fujimoto expressly criticizes this practice (Fujimoto,

col. 2, l. 65- col. 3, l. 2, col. 14, ll. 9-21) and, for the reasons stated above, would discourage one of ordinary skill in the art from following the path described in Applicants' disclosure. Therefore, claim 30 is believed to be allowable over Fujimoto in view of Porter.

d. Claim 38 Stands Independently

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 38 requires, *inter alia*, a "video graphics integrated circuit comprising: a frame buffer memory maintaining video data having a first format and graphics data having a second format . . . ." (Specification, claim 38, emphasis added.) Applicants respectfully note that claim 38 explicitly recites a frame buffer having, as indicated above, the ability to store video data and graphics data. In contrast, Fujimoto expressly criticizes this practice (Fujimoto, col. 2, l. 65- col. 3, l. 2, col. 14, ll. 9-21) and, for the reasons stated above, would discourage one of ordinary skill in the art from following the path described in Applicants' disclosure. Therefore, claim 38 is believed to be allowable over Fujimoto in view of Porter.

2. THE COMBINATION WOULD MODIFY FUJIMOTO IN A MANNER UNSATISFACTORY FOR ITS INTENDED PURPOSE AND ALSO RESULT IN REDUNDANT OPERATIONS AND STRUCTURE

Federal Circuit case law holds that if a prior art's teachings are modified such that the result renders the disclosed device inoperable for its intended purpose, the reference teaches away from the proposed modification. *In re Gordon*, 733 F.2d 900, 902, 221 U.S.P.Q. 1127 (Fed. Cir. 1984). In *Gordon*, the patent applicant claimed a blood filter assembly for use in medical procedures to remove foreign material from blood. *Id.* at 900, at 1126. The PTO rejected the claim as obvious over modified prior art where the sole reference disclosed a gravity-dependent, liquid strainer designed to separate dirt and water from oils. *Id.* at 901, at 1127. The Federal Circuit observed that after "a fair reading" of the reference, the PTO's proposed modification of the prior art apparatus would operate such that the device would be a poor filter. *Id.* at 902, at 1127. More particularly, if the prior art strainer was turned upside down as taught by the PTO, the oils would be trapped inside the filter, water would freely flow, dirt would, in time, clog the screen and a new drain valve element would be required at the new

bottom of the device. *Id.* As a result, the reference taught away from the applicant's claimed invention. *Id.*

a. Claims 3, 7, 9, 14, 17 and 19 Stand Together with Claim 4

Assuming, *arguendo*, that a frame buffer such as the one described by Porter was substituted for the source DVD-ROM 100 in Fujimoto as alleged in the Final Office Action, the resulting apparatus would be inoperable for its intended purpose and would render the separate graphics VRAM 103 employed by Fujimoto's system redundant. As indicated *supra*, an object of Fujimoto's disclosure is to display combined video and graphics data, initially stored on a source DVD-ROM 100, on a television monitor 200 using a separate VRAM 103 for graphics data instead of a frame buffer or other video memory. (Fujimoto, col. 3., ll. 13-19.) However, the substitution of a frame buffer for the source DVD-ROM 100 would not only create a system without a source of video or graphics data but would also render key portions of his structure redundant and therefore, useless. Hence, Fujimoto teaches away from the substitution of a frame buffer for the source DVD-ROM 100.

In the present case, Applicants claim, *inter alia*, "a single frame buffer operably coupled to the graphics scaler and to the video scaler." (Specification, claim 4, emphasis added.) By definition, a buffer may be said to 'buffer' information from another source for subsequent transmission to another entity or location. A frame buffer, therefore, inherently has read/write capabilities, but cannot serve as the source of the information it stores. (*See e.g.*, Specification at 5, ll. 3-6, Figs. 1, 2) In contrast, the Examiner in Final Office Action stated, *inter alia*, that it would have been obvious to substitute a frame buffer, as described in Porter, with the DVD-ROM 100 of Fujimoto. (Final Office Action at 3.)

However, if one were to substitute a frame buffer for the DVD-ROM 100 as suggested in the Final Office Action, the image display control system of Fujimoto would have nothing to display. Fujimoto describes the DVD-ROM 100 as a necessary element of the disclosure because it is the only source of video and graphics data for the display system. (Fujimoto, col. 1, ll. 28-40; col. 3, ll. 13-19, Fig. 1.) Such a substitution would render the Fujimoto apparatus inoperable for its intended purpose of displaying combined video and graphics data from a DVD in the same manner that the gravity-dependent, liquid strainer in *Gordon* was rendered

inoperable for filtering oils from water if turned upside down so as to function as the claimed blood filter assembly. *Gordon*, 733 F.2d at 902, 221 U.S.P.Q.2d at 1127. Therefore, Fujimoto teaches away from the alleged combination with Applicants' claimed subject matter.

Moreover and as also explained *infra*, the substitution of a frame buffer for the DVD-ROM 100 as suggested in the Final Office Action would render VRAM 103 and main memory 13 redundant and undesirable because a frame buffer as a read/write memory would perform the same functions as VRAM 103 and main memory 13 with respect to graphics data 100G and video data 100B, respectively. Such a substitution would run counter to the explicit teachings found in Fujimoto. As described above, Fujimoto clearly discourages the use of a large video memory to store both graphics data 100G and video data 100B and instead eliminates it by using a dedicated graphics VRAM 103 and main memory to store encoded video. Therefore, the Examiner's suggestion creates a situation where Fujimoto teaches not to use large video memory, yet it is somehow obvious to substitute the frame buffer of Porter for the source DVD-ROM 100 of Fujimoto.

For the aforementioned reasons alone, the obvious rejections with respect to claims 3, 4, 7, 9 14, 17 and 19 must be reversed.

b. Claims 22 and 26-28 Stand Together with Claim 20

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 20 requires, *inter alia*, a "method for displaying video graphics data comprising: receiving a video data stream . . . ; allocating a first block of a memory in a frame buffer for storing the video data stream . . ., receiving a graphics data stream . . ., [and] allocating a second block of a memory in a frame buffer for storing the graphics data stream . . . ." (Specification, claim 20, emphasis added.) Applicants respectfully note that claim 20 explicitly recites a frame buffer that, *inter alia*, both receives and allocates a corresponding block of memory for storing a video data stream and/or a graphics data stream. In other words, Applicants claim a frame buffer that is not the source of the data stored therein as it buffers data from another source. In contrast, Fujimoto expressly teaches that the DVD-ROM 100 is, and must be, the source of both video and graphics data as input to the display system. (Fujimoto, col. 1, ll. 28-40, col. 3 ll. 13-19, Fig. 1.) Because the

substitution of a frame buffer for the source DVD-ROM 100 would render the Fujimoto apparatus inoperable for its intended purpose of displaying combined video and graphics data from a DVD, Fujimoto necessarily teaches away from Applicants' claimed subject matter. Therefore, claims 20, 22 and 26-28 are believed to be allowable for at least the same reasons that claims 3, 4, 7, 9, 14, 17 and 19 are allowable over Fujimoto in view of Porter.

c. Claim 30 Stands Independently

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 30 requires, *inter alia*, a "video graphics integrated circuit comprising: a frame buffer, wherein the frame buffer stores video data and graphics data . . . ." (Specification, claim 30, emphasis added.) Applicants respectfully note that claim 30 explicitly recites a frame buffer with similar properties as the frame buffer in claim 4. In other words, the frame buffer inherently has read/write capabilities, but cannot serve as the source of the information it stores. (*See e.g.*, Specification at 5, ll. 3-6, Figs. 1-2.) In contrast, Fujimoto expressly teaches that the DVD-ROM 100 is, and must be, the source of both video and graphics data as input to the display system. (Fujimoto, col. 1, ll. 28-40, col. 3 ll. 13-19, Fig. 1.) Because the substitution of a frame buffer for the source DVD-ROM 100 would render the Fujimoto apparatus inoperable for its intended purpose of displaying combined video and graphics data from a DVD, Fujimoto necessarily teaches away from Applicants' claimed subject matter. Therefore, claim 30 is believed to be allowable over Fujimoto in view of Porter.

d. Claim 38 Stands Independently

Applicants respectfully reassert the relevant remarks made above with respect to claims 3, 4, 7, 9, 14, 17 and 19. As indicated in Applicants' specification, claim 38 requires, *inter alia*, a "video graphics integrated circuit comprising: a frame buffer memory maintaining video data having a first format and graphics data having a second format . . . ." (Specification, claim 38, emphasis added.) Applicants respectfully note that claim 38 explicitly recites a frame buffer with similar properties as the frame buffer in claim 4. In other words, the frame buffer inherently has read/write capabilities, but cannot serve as the source of the information it stores. (*See e.g.*, Specification at 5, ll. 3-6, Figs. 1-2.) In contrast, Fujimoto expressly teaches that the

DVD-ROM 100 is, and must be, the source of both video and graphics data as input to the display system. (Fujimoto, col. 1, ll. 28-40, col. 3 ll. 13-19, Fig. 1.) Because the substitution of a frame buffer for the source DVD-ROM 100 would render the Fujimoto apparatus inoperable for its intended purpose of displaying combined video and graphics data from a DVD, Fujimoto necessarily teaches away from Applicants' claimed subject matter. Therefore, claim 38 is believed to be allowable over Fujimoto in view of Porter.

B. THE EXAMINER HAS PROVIDED ONLY BROAD, CONCLUSORY STATEMENTS OF A MOTIVATION TO COMBINE THE REFERENCES AND THEREFORE HAS NOT SATISFIED THE *PRIMA FACIE* CASE OF OBVIOUSNESS

As stated *supra*, the PTO bears the initial burden of presenting a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1998). Absent a proper *prima facie* case, an application is entitled to issuance provided that the other provisions of the Patent Act are satisfied. *Rouffett*, 149 F.3d at 1355, 47 U.S.P.Q.2d at 1455. The *prima facie* case is only satisfied when the PTO demonstrates, *inter alia*, that the prior art teaches, suggests or motivates a person having ordinary skill in the art to combine the references to make or carry out the claimed subject matter. *In re Vaeck*, 947 F.2d 488, 493, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

Case law is clear: the use of an applicant's disclosure as a template or blueprint for combining references is impermissible, hindsight analysis – a reversible, legal error. *Gorman*, 933 F.2d at 987, 18 U.S.P.Q.2d at 1888; *see also Fine*, 837 F.2d at 1075, 5 U.S.P.Q.2d at 1600 (stating that without adherence to this prerequisite, "the insidious effect of a hindsight syndrome . . . [allows] . . . that which only the inventor taught [to be] used against the teacher"). Therefore, the motivation to combine references must be explicitly or implicitly found in either the prior art references, in the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved such that one of ordinary skill in the art would look to the cited references to find a solution. *Ruiz*, 234 F.3d at 665, 57 U.S.P.Q.2d at 1167. Regardless, the evidence of such a motivation must be garnered from the prior art as a whole in such a manner to suggest the desirability and obviousness of making the combination. *Ecolochem Inc. v. S. Cal. Edison*, 227 F.3d 1361, 1372, 56 U.S.P.Q.2d 1065, 1073 (Fed. Cir. 2000); *see also In re Gorman*, 933 F.2d 982, 987, 18 U.S.P.Q.2d 1885, 1888 (Fed. Cir. 1991) (holding that the references themselves, in

their appropriate context, must provide the motivation); *see also Ex parte Clapp*, 227 U.S.P.Q. 972, 973 (B.P.A.I. 1985) (noting that the PTO must do more than selectively pick and choose elements in the prior art to render a claim obvious).

In this context, the Federal Circuit recently held in *Karsten Manuf. Corp. v. Cleveland Golf Co.* that, *inter alia*, conflicting prior art cannot, in themselves, be used as a motivation to combine references. 242 F.3d 1376, 1385, 58 U.S.P.Q.2d 1286, 1293 (Fed. Cir. 2001). That is, where the prior art discloses conflicting teachings and lacks a motivation to combine references, the Court noted that only improper, hindsight analysis would allow an artisan to selectively combine the necessary elements from the references. *Id.* Similarly, the fact that a device might be capable of being modified to operate in the claimed manner will not defeat patentability unless there is a suggestion or motivation to combine the references. *In re Mills*, 916 F.2d 680, 682, 16 U.S.P.Q.2d 1430, 1432 (Fed. Cir. 1990) (citing *Gordon*, 733 F.2d at 902, 221 U.S.P.Q. at 1127).

While the PTO may rely on explicit or implicit knowledge, the objective showing that one of ordinary skill in the art would have been motivated to select the references and combine them "must be clear and particular." *Dembiczak*, 175 F.3d at 999, 50 U.S.P.Q.2d at 1617, *Fine*, 837 F.2d at 1074, 5 U.S.P.Q.2d at 1598. Broad, conclusory statements alone are not sufficient to establish this showing. *Id.* "Particular findings must be made as to the reason [a] skilled artisan . . . would have selected [the prior art] components for combination in the manner claimed." *Kotzab*, 217 F.3d at 1371, 55 U.S.P.Q.2d at 1317. In fact, this Board has held before that when an applicant claims a new combination of elements, the PTO must present a convincing line of reasoning as to why an artisan would find the claim obvious in light of the prior art. *Clapp*, 227 U.S.P.Q. at 973.

1. CLAIMS 3, 7, 9, 14, 17 AND 19 STAND TOGETHER WITH CLAIM 4

In addition to the ways in which Fujimoto teaches away from the alleged combination with Porter as described above, Applicants further submit that the Examiner has submitted bald, conclusory explanations for combining the references without providing sufficient factual support and while ignoring the fact that: (1) Fujimoto, in every instance, refers to the source DVD-ROM 100 as read-only memory source of information and therefore would not be

motivated to substitute a memory capable of reading and writing; (2) Porter stands for the proposition that memory 10, used to store, *inter alia*, pre-rendered graphics images and video data, may be a DVD Memory but is preferably a frame buffer, and does not stand for the proposition that a DVD Memory can always be substituted for a frame buffer; and (3) the substitution of a frame buffer in place of the DVD-ROM 100 would render the VRAM 103 and main memory 13 redundant and undesirable. Moreover, the substitution would conflict with a principal Fujimoto teaching that no large video memories should be used in the display system. For these reasons, the PTO has failed to establish a *prima facie* case of obviousness. Without a *prima facie* case, the claims are respectfully submitted for allowance. *Vaeck*, 947 F.2d at 493, 20 U.S.P.Q.2d at 1442.

In the Final Office Action, the Examiner stated, *inter alia*, that "it would have been obvious to one of skill in the art to include Porter's teaching of a single frame buffer memory in the disclosure of Fujimoto because Fujimoto provides memory read and write transactions from the CPU (col. 10, ll. 47-57), as does a frame buffer, whereas Porter's provision for memory allows for a single memory device that preferably [sic] a frame buffer that may be substituted for a DVD memory." (Final Office Action at 3.) Applicants respectfully characterize this motivation statement as bald and conclusory. While Fujimoto does, in fact, teach that CPU 11 may perform read and write commands to for instance, main memory 13 and mask ROM 14 (Fujimoto, Fig. 8), Applicants submit that the source DVD-ROM 100 is a read-only memory and serves as the source of the video and graphics data as described *supra*. Therefore, Fujimoto alone provides no motivation for one of ordinary skill in the art to replace the read-only source DVD-ROM 100 with a frame buffer merely because the system's CPU 11, like all system CPU's, is capable of performing read and write commands to other memory elements. Additionally, because the CPU 11 in Fujimoto actually reads information from the source DVD-ROM 100 and writes only encoded video data 100B to main memory 13 and then reads it for MPEG2 decoding via MPEG2 decoder 102, there is no factual statement or support given for the alleged combination to apparent redesign of Fujimoto. In other words, there is no reason given as to why one or ordinary skill in the art would, in effect, use two sets of buffer memory (both the main memory and frame buffer) to store the same information as the Final Office Action inherently suggests.

Moreover, the Porter reference alone does not supply the necessary motivation to substitute a frame buffer for the source DVD-ROM 100. As taught by Porter, a memory 10 may include any device that stores digital information. (Porter, col. 2, ll. 51-52.) Porter also states that while the preferred embodiment of memory 10 is "a dynamic random access memory that is utilized as a frame buffer within the video graphics circuit" (Porter, col. 2, ll.53-55), the memory 10 may also be, *inter alia*, DVD memory (Porter, col. 2, ll. 46-51). While this cited portion of Porter indicates that the memory 10 may be a frame buffer or a DVD memory, Porter does not teach that a frame buffer can be substituted for a source DVD memory. As explained above, a frame buffer is not analogous to a read-only source DVD memory in that a frame buffer inherently acts as a 'buffer'; it has read and write abilities. That is to say, a frame buffer is not designed to be the source of audio data or graphics data. (*See e.g.*, Specification, Fig. 1.) Because DVD memories are often affiliated with the source of audio and video data, as clearly indicated throughout Fujimoto, it is difficult to find a clear and particular motivation within Porter to automatically equate a frame buffer with a source DVD-ROM 100. Because the Examiner has failed to provide this motivation and motivation to redesign Fujimoto, the PTO has failed to demonstrate a *prima face* case of obviousness.

Lastly, and as mentioned *supra*, the substitution of a frame buffer for the DVD-ROM 100 as suggested in the Final Office Action would render VRAM 103 and main memory 13 redundant and undesirable because a frame buffer as a read/write memory would perform the same functions as VRAM 103 and main memory 13 with respect to graphics data 100G and video data 100B, respectively. Such a substitution would run counter to the explicit teachings found in Fujimoto. As described above, Fujimoto clearly discourages the use of a large video memory to store both graphics data 100G and video data 100B and instead eliminates it by using a dedicated graphics VRAM 103 and main memory to store encoded video. Therefore, the Examiner's suggestion creates a situation where Fujimoto teaches not to use large video memory, yet it is somehow obvious to substitute the frame buffer of Porter for the source DVD-ROM 100 of Fujimoto. Without a clear and particular motivation to combine Fujimoto and Porter, such conflicting teachings among the prior art references indicates that the PTO improperly relied on hindsight analysis to reconstruct Applicants' claimed subject matter. 242 F.3d at 1385, 58 U.S.P.Q.2d at 1293.

Because the Examiner has merely submitted bald and conclusory statements regarding an alleged motivation to substitute the frame buffer of Porter with the source DVD-ROM 100 of Fujimoto, the Final Office Action has failed to make clear and particular findings as to the reason an artisan would combine the two references. This error allowed the examiner to use the Applicants' own disclosure as a blueprint for combining two seemingly-incompatible references which is improper. *Fine*, 837 F.2d at 1075, 5 U.S.P.Q.2d at 1600. Moreover, the lone fact that the a prior art reference might be physically capable of being modified, with hindsight analysis, so as to read on Applicants' claimed subject matter, does not support a motivation to combine the teachings of Fujimoto and Porter. *Mills*, 916 F.2d at 682, 16 U.S.P.Q.2d at 1432. In any event, the language set forth in the Final Office Action fails to specify how or why Fujimoto would be modified to actually work as alleged. Because the Examiner has merely submitted broad statements regarding the motivation to combine Fujimoto and Porter, and has offered little relevant objective support for the Examiner's statement, claims 3, 4, 7, 9, 14, 17 and 19 are believed to be in proper condition for allowance.

2. CLAIMS 22 AND 26-28 STAND TOGETHER WITH CLAIM 20

Applicants respectfully reassert the relevant remarks made with respect to claims 3, 4, 7, 9, 14, 17 and 19 and submit that claims 20, 22 and 26-28 are in proper condition for allowance because, *inter alia*, the Examiner has failed to support a *prima facie* case of obviousness.

3. CLAIM 30 STANDS INDEPENDENTLY

Applicants respectfully reasserts the relevant remarks made with respect to claims 3, 4, 7, 9, 14, 17 and 19 and submit that claim 30 is in proper condition for allowance because, *inter alia*, the Examiner has failed to support a *prima facie* case of obviousness.

4. CLAIM 38 STANDS INDEPENDENTLY

Applicants respectfully reassert the relevant remarks made with respect to claims 3, 4, 7, 9, 14, 17 and 19 and submit that claim 38 is in proper condition for allowance because, *inter alia*, the Examiner has failed to support a *prima facie* case of obviousness.

C. THE OBVIOUS REJECTIONS MUST BE REVERSED SINCE THE EXAMINER HAS FAILED TO DEMONSTRATE THAT THE PRIOR ART TEACHES OR SUGGESTS EACH CLAIM LIMITATION

As stated *supra*, a finding of obviousness requires a demonstration that the prior art teaches or suggests each claim limitation. *See Thrift*, 398 F.3d at 1366, 63 U.S.P.Q.2d at 2008 (reversing a Board's adverse decision on obviousness because the prior art references failed to support each claim limitation). As logic demands, each word within a claim must be properly evaluated. *Wilson*, 424 F.2d at 1385, 165 U.S.P.Q. at 496. If the prior art as evaluated in its entirety, *Kotab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1370, does not teach or suggest each claim limitation, the claim cannot be said to be obvious in light of the prior art, LESTER HORWITZ, PATENT OFFICE RULES AND PRACTICE: MANUEL OF PATENT EXAMINING PROCEDURE § 2143.03 (8th ed. 2003).

1. CLAIM 15 STANDS TOGETHER WITH CLAIM16

Applicants respectfully reassert the remarks made above with respect to claim 4. Additionally, Applicants submit that because claim 15 depends upon claim 4, claim 15 is allowable for at least the same reasons that claim 4 is allowable. *See e.g., Fine*, 837 F.2d at 1076, 5 U.S.P.Q.2d at 1600 (holding that if an independent claim is nonobvious under 35 U.S.C. § 103(a), then any claim depending thereupon is also nonobvious). Claim 15, however, is additionally allowable because it contains other novel and non-obvious elements that are not otherwise present in claim 4 or in the prior art.

For instance, claim 15 recites: "The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling ratio, wherein the preferred video scaling ratio is based on the ratio between the video images in the first format and the output video image." (Specification, claim 15, emphasis added.) The Final Office Action cites column 2, lines 46-64 and column 3, lines 18-35 of Fujimoto as rendering the above claim language obvious. (Final Office Action at 5.)

In contrast to the claimed subject matter where, *inter alia*, "the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling" and where "the preferred video scaling ratio is based on the ratio

between the video images in the first format and the output video image" (Specification, claim 15, emphasis added), the cited portions of Fujimoto only discuss some of the many objects of the reference's disclosure. Applicants are unable to identify where in the cited portions Fujimoto teaches or suggests the aforementioned claim limitations. Consequentially, claim 15 stands in proper condition for allowance.

Applicants respectfully reassert the relevant remarks made above with respect to claim 15. In the Final Office Action, the Examiner rejected claim 16 for the same reasons as claim 15. (Final Office Action at 4.) Because claim 16 corresponds to, "the display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred graphics scaling ratio, wherein the preferred graphics scaling ratio is based on the ratio between the graphic images in the first format and the output graphic image" (Specification, claim 16, emphasis added), the claim is in proper condition for allowance for the same reasons that the subject matter of claim 15 is allowable over Fujimoto and Porter.

2. CLAIM 29 STANDS TOGETHER WITH CLAIM 18

Applicants respectfully reassert the remarks made above with respect to claims 4 and 20. Additionally, Applicants submit that because claims 18 and 29 respectively depend upon claims 4 and 20, claims 18 and 29 are allowable for at least the same reasons that claims 4 and 20 are allowable. *See e.g., Fine*, 837 F.2d at 1076, 5 U.S.P.Q.2d at 1600 (holding that if an independent claim is nonobvious under 35 U.S.C. § 103(a), then any claim depending thereupon is also nonobvious). Claims 18 and 29, however, are additionally allowable because they contains other novel and non-obvious elements that are not otherwise present in claims 4 and 20 or in the prior art.

For instance, claim 18 recites: "The display engine of claim 4 further comprises a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream." (Specification, claim 18, emphasis added.) The Final Office Action cites to Figs. 1, 17, column 15, lines 10, et. seq. of Fujimoto as rendering the above claim language obvious. (Final Office Action at 5.)

In contrast to the claimed subject matter where the display engine further comprises, *inter alia*, a graphics decompression block operably coupled to the graphics scaler (Specification, claim 18), the cited portion of Fujimoto, as best understood, teaches the process of reading the graphics data stored in VRAM 103. Because the cited reference does not teach or suggest any portion of Applicants' claimed subject matter, claims 18 and 29 stand in proper condition for allowance.

D. CLAIMS 12-13 AND 24-25 ARE ALLOWABLE BECAUSE THE PRIOR ART DOES NOT TEACH OR SUGGEST THE CLAIMED SUBJECT MATTER

As explained *supra*, if the prior art as evaluated in its entirety, *Kotab*, 217 F.3d at 1370, 55 U.S.P.Q.2d at 1370, does not teach or suggest each claim limitation, the claim cannot be said to be obvious in light of the prior art, LESTER HORWITZ, PATENT OFFICE RULES AND PRACTICE: MANUEL OF PATENT EXAMINING PROCEDURE § 2143.03 (8th ed. 2003). Because the subject matter in claims 12-13 and 24-25 is not taught or suggested by the combination of Fujimoto and Porter, or any prior art cited by the Examiner throughout prosecution, the claims stand in proper condition for allowance.

1. CLAIMS 24 AND 25 STAND TOGETHER WITH CLAIMS 12 AND 13, RESPECTIVELY

Applicants respectfully reassert the remarks made above with respect to claim 4. Additionally, Applicants submit that because claims 12 and 13 depend upon claim 4, claims 12 and 13 are allowable for at least the same reasons that claim 4 is allowable. *See e.g., Fine*, 837 F.2d at 1076, 5 U.S.P.Q.2d at 1600 (holding that if an independent claim is nonobvious under 35 U.S.C. § 103(a), then any claim depending thereupon is also nonobvious). Claims 12 and 13, however, are additionally allowable because they contain other novel and non-obvious elements that are not otherwise present in claim 4 or in the prior art.

For instance, claim 12 recites: "The display engine of claim 4 further comprises a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream." (Specification, claim 12, emphasis added.) Similarly, claim 13 further recites "a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream." (Specification, claim 13, emphasis added.)

In the Office Action mailed May 21, 2003 ("2003 Office Action"), the Examiner rejected claims 12-13 and 24-25 under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto in view of U.S. Patent No. 6,189,0164 (MacInnis). (2003 Office Action at 5.) Additionally, the Examiner explicitly stated that Fujimoto fails to disclose a graphics or video flicker removal block. (2003 Office Action at 7). After responding to the 2003 Office Action by way of an amendment and response, the Examiner withdrew the rejection with respect to claims 12-13 and 24-25 in the Office Action mailed March 2, 2004 ("2004 Office Action"). (2004 Office Action at 9.) More specifically, the 2004 Office Action stated that the aforementioned claims "are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." (2004 Office Action at 9.) As of the Final Office Action, claims 12-13 and 24-25 were objected to for the same reasons listed above. (Final Office Action at 9.)

In other words, the Examiner was unable to find, in any cited prior art, a teaching or suggestion that would render obvious Applicants' claimed subject matter. Because the combination of the cited prior art references do not teach or suggest a "graphics flicker removal block" or a "video graphics removal block" as claimed, Applicants respectfully submit claims 12-13 and 24-25 for allowance.

IX. Conclusion

For the reasons advanced above, Appellants submit that the Examiner erred in rejecting pending claims 2-4, 6-11, 14-23, 26-30 and 38 and respectfully request reversal of the decision of the Examiner.

Respectfully submitted,

Date: March 25, 2005

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Claims on Appeal

Claim 2: The video graphics display engine of claim 4 wherein the video graphics display engine allocates a size of the first memory block of the single frame buffer and a size of the second memory block of the single frame buffer based on needs of the video data and the graphics data, respectively, and wherein the video graphics display further comprises a controller operably coupled to the video scaler and the graphics scaler, wherein the controller provides control information to the video scaler and the graphics scaler, wherein scaling operations of the video scaler and the graphics scaler utilize the control information.

Claim 3: The video graphics display engine of claim 2, wherein the merging block is operably coupled to the controller, wherein the merging block receives merging control information from the controller, wherein the merging control information is used with the scaled video stream data and the scaled graphics stream to produce the video graphics output stream.

Claim 4: A video graphics display engine comprising:

a video scaler adapted to receive a video data stream in a first format, wherein the video scaler scales video images in the video data stream based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive a graphics data stream in a second format,

wherein the graphics scaler scales graphics images in the graphics data stream based on a ratio between the graphics images in the second format and an output graphics image to produce a scaled graphics stream;

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce a video graphics output stream; and

a single frame buffer operably coupled to the graphics scaler and to the video scaler, the single frame buffer further comprises a first memory block and a second memory block, wherein the stream of video data is fetched from the first memory block and the stream of graphics data is fetched from the second memory block.

Claim 6: The display engine of claim 4, wherein the controller further comprises a video controller operably coupled to a graphics controller,

wherein the video controller is operably coupled to the video scaler, wherein the video controller provides a first portion of the control information to the video scaler,

wherein the graphics controller is operably coupled to the graphics scaler, wherein the graphics controller provides a second portion of the control information to the graphics scaler, and

wherein the video controller and the graphics controller are synchronized.

Claim 7: The display engine of claim 4, wherein the merging block performs an alpha blend operation on the scaled video stream and the scaled graphics stream to produce the video graphics output stream.

Claim 8: The display engine of claim 4 further comprises a digital to analog converter operably coupled to the merging block, wherein the digital to analog converter converts the video graphics output stream to an analog display signal.

Claim 9: The display engine of claim 4 further comprises a display driver operably coupled to the merging block, wherein the display driver is adapted to receive the video graphics output stream in digital format, wherein the display driver formats the video graphics output stream in a display compatible format.

Claim 10: The display engine of claim 4 further comprises a display driver operably coupled to the video scaler, wherein the display driver is adapted to receive the scaled video stream and produce a video display output based on the scaled video stream.

Claim 11: The display engine of claim 4 further comprises a display driver operably coupled to the graphics scaler, wherein the display driver is adapted to receive the scaled graphics stream and produce a graphics display output based on the scaled graphics stream.

Claim 12: The display engine of claim 4 further comprises a graphics flicker removal block operably coupled to the graphics scaler, wherein the graphics flicker removal block removes flicker from the scaled graphics stream.

Claim 13: The display engine of claim 4 further comprises a video flicker removal block operably coupled to the video scaler, wherein the video flicker removal block removes flicker from the scaled video stream.

Claim 14: The display engine of claim 4 further comprises a plurality of graphics scalers, wherein each of the plurality of graphics scalers receives the graphics data stream and scales the graphics images in the graphics data stream based on a ratio between the graphics images in the second format and a corresponding output graphics image to produce a corresponding scaled graphics stream.

Claim 15: The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred video scaling ratio, wherein the preferred video scaling ratio is based on the ratio between the video images in the first format and the output video image.

Claim 16: The display engine of claim 4, wherein the merging block further comprises circuitry which configures a pixel rate of the video graphics output stream to produce a preferred graphics scaling ratio, wherein the preferred graphics scaling ratio is based on the ratio between the graphics images in the second format and the output graphics image.

Claim 17: The display engine of claim 4 further comprises a video decompression block operably coupled to the video scaler, wherein the video decompression block receives a

compressed stream of video data and decompresses the compressed stream of video data to produce the video data stream.

Claim 18: The display engine of claim 4 further comprises a graphics decompression block operably coupled to the graphics scaler, wherein the graphics decompression block receives a compressed stream of graphics data and decompresses the compressed stream of graphics data to produce the graphics data stream.

Claim 19: The display engine of claim 4, wherein the video data stream is a decoded MPEG data stream.

Claim 20: A method for displaying video graphics data comprising:

receiving a video data stream, wherein the video data stream includes video data in a first format;

allocating a first block of a memory in a frame buffer for storing the video data stream, the allocating based upon memory needs of the video data stream;

receiving a graphics data stream, wherein the graphics data stream of includes graphics data in a second format;

allocating a second block of the memory in a frame buffer for storing the graphics data stream, the allocating based upon memory needs of the graphics data stream;

scaling the video data based on a ratio between the first format and a selected video format to produce a scaled video stream;

scaling the graphics data based on a ratio between the second format and a selected graphics format to produce a scaled graphics stream; and

merging the scaled video stream and the scaled graphics stream to produce a video graphics output stream.

Claim 21: The method of claim 20, wherein scaling the video data further comprises scaling the video data based on video data control information, and wherein scaling the graphics data further comprises scaling the graphics data based on graphics data control information.

Claim 22: The method of claim 20, wherein merging further comprises receiving merging control information, wherein the merging control information is used in merging scaled video stream am and the scaled graphics stream to produce the video graphics output stream.

Claim 23: The method of claim 20, further comprises converting the video graphics output stream to an analog format.

Claim 24: The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled video stream.

Claim 25: The method of claim 20, wherein scaling the video data further comprises removing the flicker from the scaled graphics stream.

Claim 26: The method of claim 20, wherein scaling the video data further comprises scaling the video data based on the first format and a plurality of selected video formats to produce a plurality of scaled video streams.

Claim 27: The method of claim 20, wherein scaling the graphics data further comprises scaling the graphics data based on the first format and a plurality of selected graphics formats to produce a plurality of scaled graphics streams.

Claim 28: The method of claim 20, wherein receiving the video data stream further comprises receiving the video data stream in a compressed format, wherein the video data stream is decompressed prior to scaling.

Claim 29: The method of claim 20, wherein receiving the graphics data stream further comprises receiving the graphics data stream in a compressed format, wherein the graphics data stream is decompressed prior to scaling.

Claim 30: A video graphics integrated circuit comprising:

a frame buffer, wherein the frame buffer stores video data and graphics data;

a video scaler operably coupled to the frame buffer, wherein the video scaler scales the video data to produce a scaled video stream;

a graphics scaler operably coupled to the frame buffer, wherein the graphics scaler scales the graphics data to produce a scaled graphics stream; and

a merging block operably coupled to the video scaler and the graphics scaler, wherein the merging block combines the sealed video data stream and the graphics data stream to produce a video graphics output stream.

Claim 38: A video graphics display circuit, comprising:

a frame buffer memory maintaining video data having a first format and graphics data having a second format, wherein the frame buffer memory allocated to the video data and the graphics data is based upon memory needs of the video data and the graphics data;

a video scaler adapted to receive the video data, wherein the video scaler scales video images in the video data based on a ratio between the video images in the first format and an output video image to produce a scaled video stream;

a graphics scaler adapted to receive the graphics data, wherein the graphics scaler scales graphics images in the graphics data based on a ration between the graphics images in the second format and an output graphics image to produce a scaled graphics stream, the video image scaling being independent of the graphics image scaling ; and

a merging block operatively coupled to the video scaler and the graphics scaler, wherein the merging block combines the scaled video stream and the scaled graphics stream to produce an video graphics output stream.

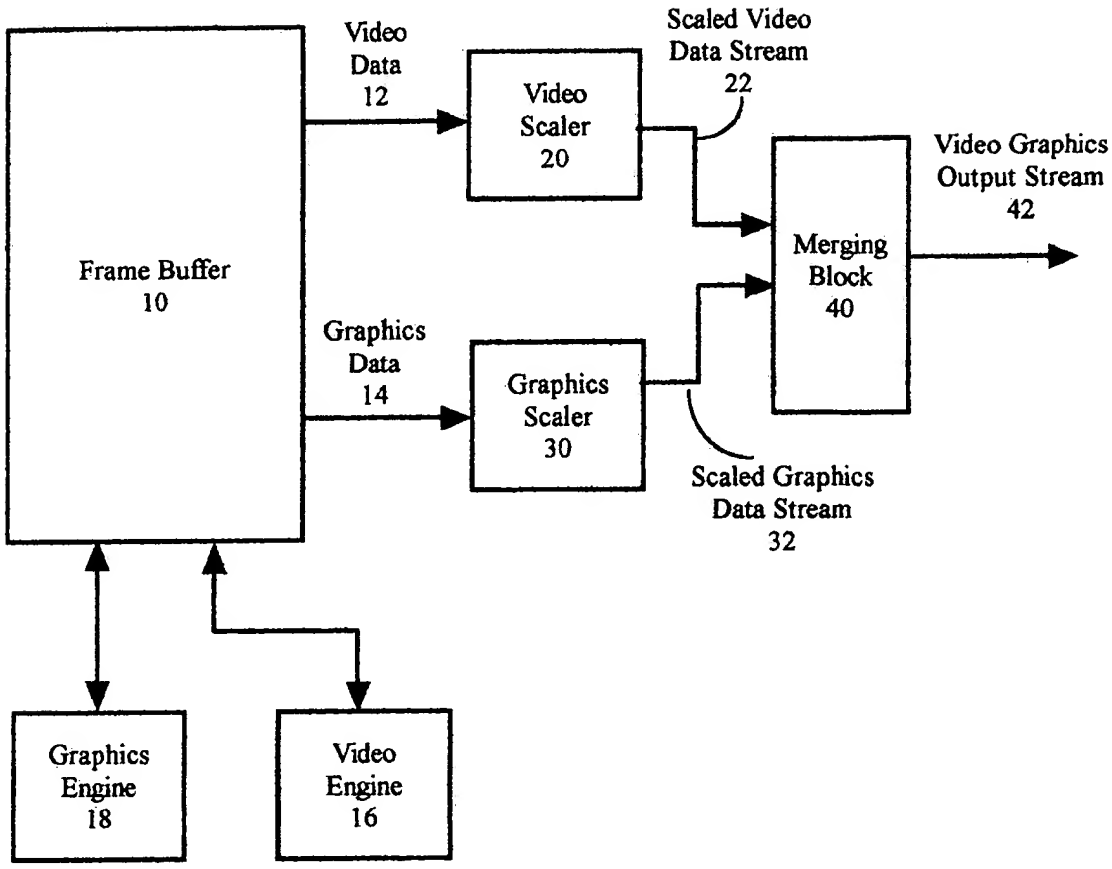

Figure 1.

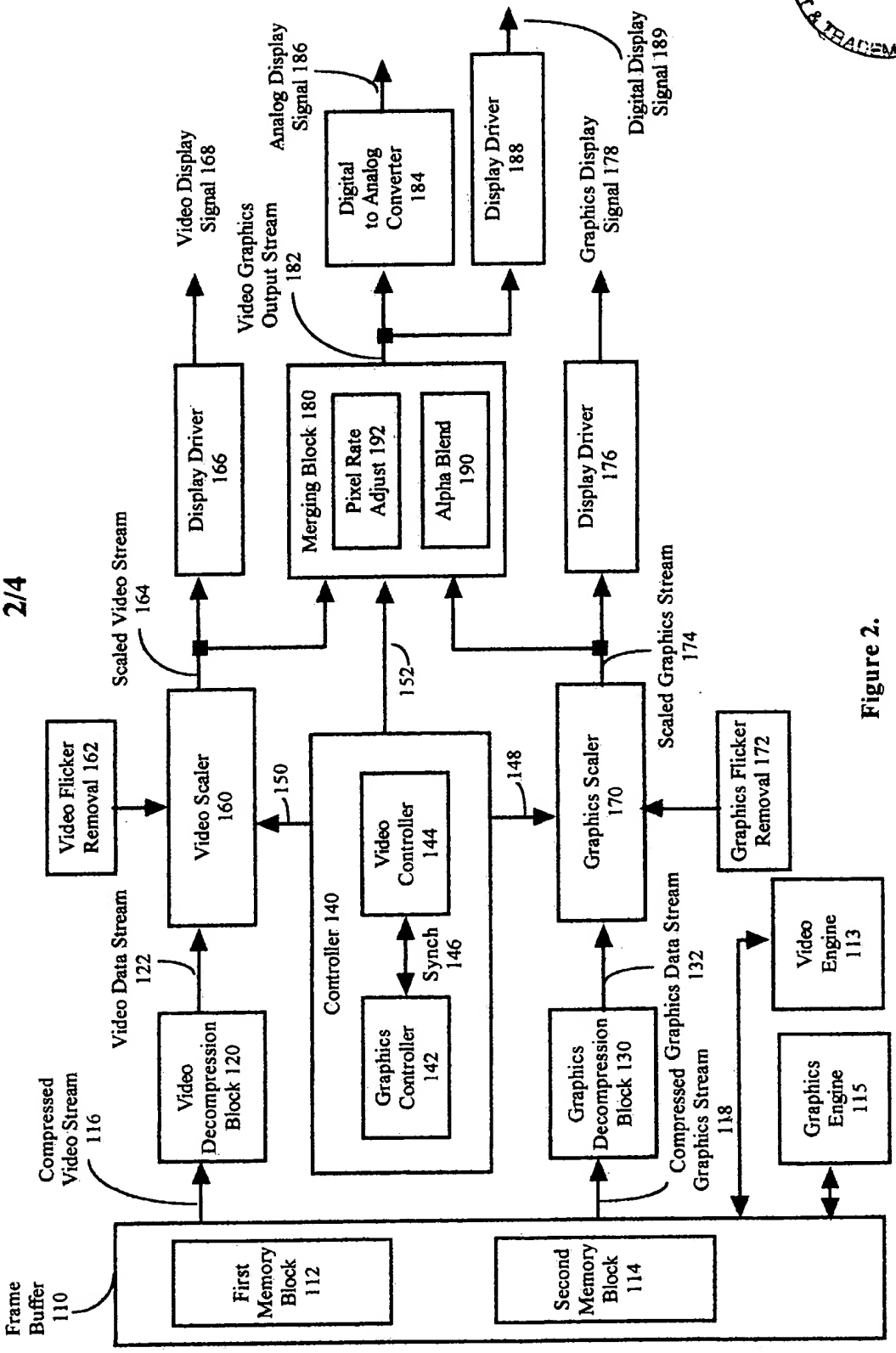

Figure 2.

Appendix C

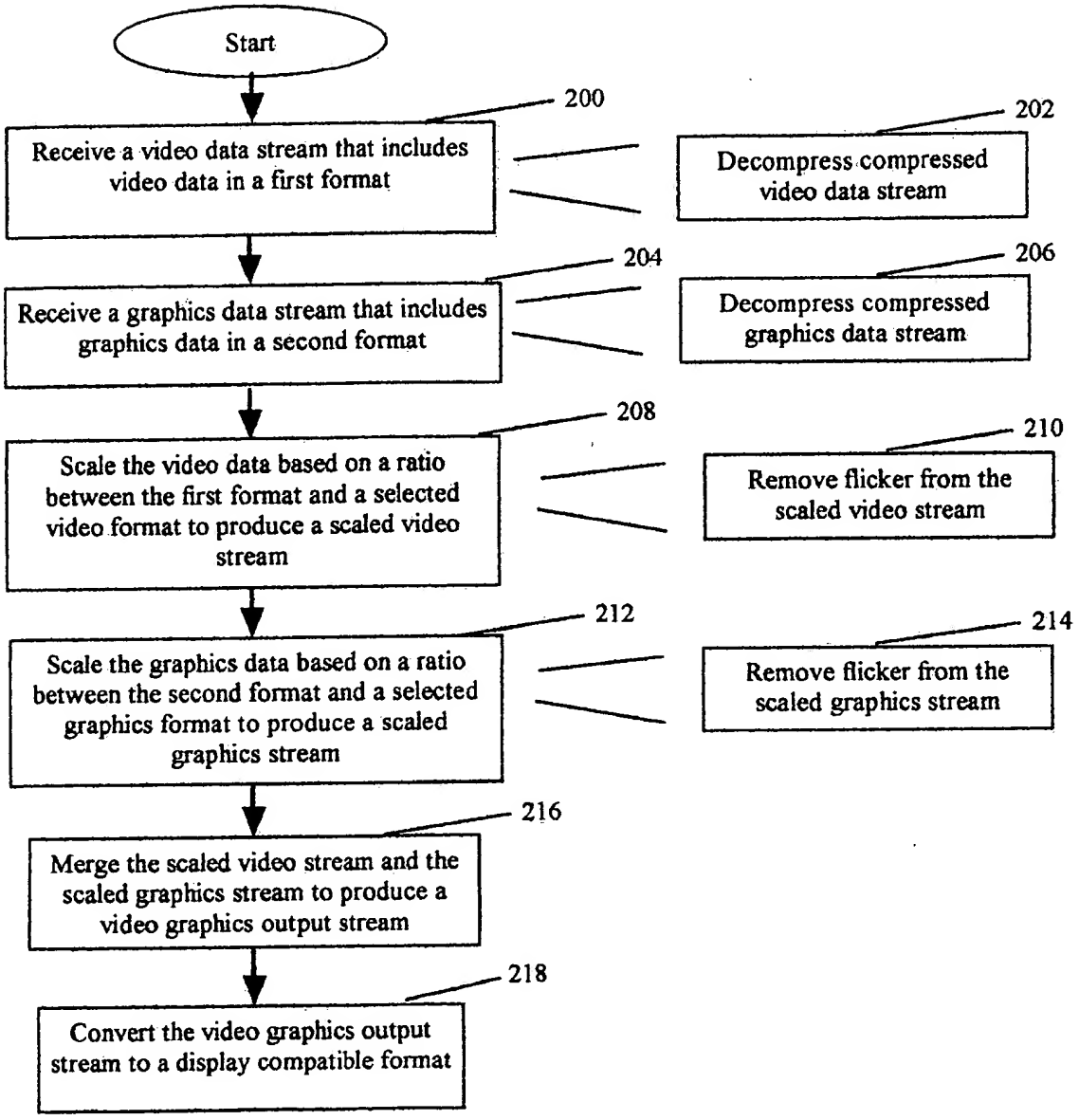

Figure 4.